

IN THE CLAIMS

Each claim of the application is set forth below with a parenthetical notation immediately following the claim number indicating the claim status. The Examiner's entry of the claim amendments under Section 1.121 is respectfully requested.

1. (CURRENTLY AMENDED) An integrated circuit device comprising:
a semiconductor substrate;
a multilevel metallization interconnect system overlying the semiconductor substrate,
each level thereof comprising first interconnect structures;

a bond pad level comprising a plurality of contact pads overlying the metallization interconnect system, one or more of the plurality of contact pads configured for connection external to the device; ~~and connected to the metallization interconnect system;~~ and

~~a ~~an~~ second interconnect structure ~~connecting~~ configured to transfer power from one or more of the plurality of contact pads connected to an external power source to a plurality of the first interconnect structures, metallization interconnect system, wherein at least a portion of the second interconnect structure configured to transfer power is disposed in the bond pad level and connected to each one of the plurality of first interconnect structures through a conductive via. extends to other regions of the semiconductor substrate away from the plurality of contact pads.~~

2. (PREVIOUSLY PRESENTED) The integrated circuit device of claim 1 wherein a material of the metallization interconnect system comprises copper.

3. (PREVIOUSLY PRESENTED) The integrated circuit device of claim 1 wherein a material of the plurality of contact pads comprises aluminum.

4. (ORIGINAL) The integrated circuit device of claim 1 wherein the plurality of contact pads are configured for connection external to the device by a bond wire attached to one or more of the plurality of contact pads.

5. (ORIGINAL) The integrated circuit device of claim 1 wherein the plurality of contact pads are configured for connection external to the device by a solder bump attached to one or more of the plurality of contact pads.

6. (PREVIOUSLY PRESENTED) The integrated circuit device of claim 1 wherein a material of the metallization interconnect system comprises copper and the plurality of contact pads comprises aluminum, further comprising a barrier material in regions of physical contact between the copper and the aluminum.

7. (CANCEL)

8. (PREVIOUSLY PRESENTED) The integrated circuit device of claim 1 wherein the metallization interconnect system further comprises substantially horizontal conductive runners and substantially vertical conductive vias interconnecting overlying and underlying conductive runners.

9. (PREVIOUSLY PRESENTED) The integrated circuit device of claim 8 wherein a material of the substantially horizontal conductive runners and the substantially vertical conductive vias comprises copper.

10. (CURRENTLY AMENDED) The integrated circuit device of claim 1 further comprising a passivation layer disposed between the bond pad level and the metallization interconnect system, wherein the passivation layer is further disposed between the second interconnect structure configured to transfer power and an uppermost level of the metallization interconnect system.

11. (ORIGINAL) The integrated circuit device of claim 1 further comprising a passivation layer overlying the bond pad level.

12. (CURRENTLY AMENDED) An integrated circuit device comprising:
a multilevel metallization interconnect system, each level thereof comprising first interconnect structures;

a plurality of contact pads disposed over an uppermost level of the multilevel metallization interconnect system, one or more of the plurality of contact pads configured for connection external to the device; and

an second interconnect structure coplanar with at least one of the plurality of contact pads and electrically connected thereto, the second interconnect structure comprising a plurality of conductive elements each connected to one of the first interconnect structures through a conductive via. ~~underlying levels of the multilevel metallization interconnect system away from the plurality of contact pads.~~

13. (CURRENTLY AMENDED) The integrated circuit device of claim 12 wherein a material of the multilevel metallization interconnect system ~~one or more levels of interconnect~~ comprises copper.

14. (CURRENTLY AMENDED) The integrated circuit device of claim 12 wherein a material of the contact pads and the second interconnect structure ~~configured to connect one or more of the underlying levels~~ comprises aluminum.

15. (CURRENTLY AMENDED) The integrated circuit device of claim 12 wherein the multilevel metallization interconnect system ~~one or more levels of interconnect~~ further comprises substantially horizontal conductive runners and substantially vertical conductive vias interconnecting overlying and underlying conductive runners.

16. (PREVIOUSLY PRESENTED) The integrated circuit device of claim 15 wherein a material of the substantially horizontal conductive runners and the substantially vertical conductive vias comprises copper.

17. (WITHDRAWN) A process for forming an interconnect metallization system overlying a semiconductor substrate of an integrated circuit device, the process comprising:

forming one or more interconnect levels overlying the semiconductor substrate;

forming a bond pad level overlying the one or more interconnect levels, wherein the bond pad level comprises a plurality of contact pads each configured for connection external to the device, and an interconnect configured to transfer power from one or more of the plurality of contact pads to one or more of the underlying interconnect levels.

18. (WITHDRAWN) The process of claim 17 wherein the step of forming the bond pad level further comprises:

forming a dielectric layer overlying the one or more interconnect levels;

forming openings in the dielectric layer;

forming a conductive blanket layer overlying the dielectric layer;

forming the plurality of contact pads and the interconnect from the blanket layer, wherein the contact pads are formed in the openings and the interconnect is formed overlying the dielectric layer.

19. (WITHDRAWN) The process of claim 18 further comprising forming a barrier layer in the openings prior to forming the blanket layer.

20. (WITHDRAWN) The process of claim 17 further comprising forming a passivation layer overlying the bond pad level.

21. (WITHDRAWN) The process of claim 17 wherein the material of the one or more interconnect levels comprises copper.

22. (WITHDRAWN) The process of claim 17 wherein the material of the bond pad level comprises aluminum.

23. (WITHDRAWN) The process of claim 17 further comprising forming a plurality of conductive vias underlying the bond pad level for connecting with the one or more interconnect levels for transferring power from one or more of the plurality of contact pads to one or more of the underlying interconnect levels.

24. (WITHDRAWN) A process for forming an interconnect metallization system overlying a semiconductor substrate of an integrated circuit device, the process comprising:

forming one or more interconnect levels overlying the semiconductor substrate;

forming a bond pad level overlying the one or more interconnect levels, wherein the bond pad level comprises a plurality of contact pads each configured for connection external to the device, and an interconnect structure configured to connect one of the one or more underlying interconnect levels to another one of the one or more underlying interconnect levels.

25. (WITHDRAWN) The process of claim 24 wherein the step of forming the bond pad level further comprises:

forming a dielectric layer overlying the one or more interconnect layers;

forming openings in the dielectric layer;

forming a conductive blanket layer overlying the dielectric layer;

forming the plurality of contact pads and the interconnect structure from the blanket layer, wherein the contact pads are formed in an opening and the interconnect structure is formed overlying the dielectric layer.

26. (CURRENTLY AMENDED) The integrated circuit of claim 1 wherein at least a portion of the second interconnect structure ~~configured to transfer power~~ is disposed above one or more of the plurality of contact pads.